(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 973 148 A1

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
19.01.2000 Bulletin 2000/03

(51) Int Cl.7: **G09G 3/36**

(21) Application number: **99305537.5**

(22) Date of filing: **13.07.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **13.07.1998 JP 19699198**

(71) Applicant: **Seiko Instruments Inc.**
Chiba-shi, Chiba (JP)

(72) Inventor: **Nogawa, Shinichi**
Mihama-ku, Chiba-shi, Chiba (JP)

(74) Representative: **Sturt, Clifford Mark et al**
Miller Sturt Kenyon
9 John Street
London WC1N 2ES (GB)

(54) **Display driver circuit for liquid crystal display with generation of gradations**

(57) In a liquid crystal display circuit enabling gradation display of a pixel by using both a pulse width modulation in which a drive pulse width PW for each segment is changed stepwise and a frame modulation in which the way of outputting a drive pulse is changed stepwise for each of one pair of frames F1 to F4 of a display screen, it is controlled for each of the frames of the display screen whether or not the pulse width PW of a segment signal of each pixel is increased by a minimum fine adjustment width, so that the total density of the frames F1 to F4 has continuity and unevenness does not occur in gradation setting.

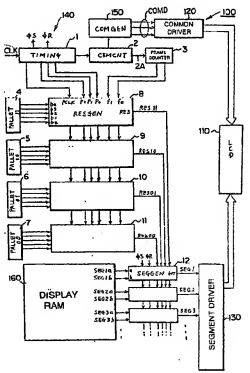

Fig.1

EP 0 973 148 A1

Description

[0001] The present invention relates to a liquid crystal display circuit for driving a liquid crystal of a portable information terminal or the like, and particularly to a liquid crystal display circuit capable of changing the tone of each pixel stepwise.

[0002] Conventionally, in order to make the tone of each pixel have gradation, as shown in Fig. 9(a), there is known a means in which for a common signal COM 1, eight pulse signals of PW = 1 to 8 with different pulse widths are prepared as segment signals for driving pixels, and a driving time is finely adjusted thereby. The means is also called a PWM (pulse width modulation) system in the sense that the pulse width of a segment signal is made variable. In this PWM system, as the variable width of the pulse width is made fine, the precision of the gradation becomes excellent, while there occurs a problem that as the variable width is made fine, the frequency of a control clock becomes high.

[0003] Then, in addition to the control of the pulse width, as shown in Fig. 9(b), there is also a system using a frame modulation as well in which the way of outputting a segment pulse is changed to xl, x2, x3, and x4 for each of a pair of frames F1, F2, F3, and F4 of a display screen so that tone control is made. Like this, in order to make the fine tone control, it is desirable to use both the pulse width modulation and the frame modulation, and this has been common as a system of gradation control.

[0004] As is understood from Fig. 9(b), the conventional way of the frame modulation is such that control is made as to whether or not a signal prepared as a segment signal is outputted in one pair of continuous frames, and such an effect can be expected that when the signal is outputted for all frames (the case of x4 in the example of Fig. 9(b)), the pixel becomes dense, and in the case where the signal is outputted for once every four frames as in the example of xl of Fig. 9(b), the pixel becomes pale.

[0005] However, since the way of the conventional frame modulation is a method of whether or not a segment signal is outputted, there has been a problem that when an attempt is made to control gradation stepwise, it lacks in continuity.

[0006] This will be described with reference to Fig. 10. In a timing diagram shown in Fig. 10(a), when the pulse width of a segment signal to be outputted is 1 (PW = 1), since it is possible to control such that one pulse is outputted or two pulses are outputted (26 to 29) in the continuous four frames (F1, F2, F3, and F4), when summing is made in the four frames, the fineness, that is, the sum of segment driving times in the four frames is continuous as 1, 2, 3, and 4. On the other hand, in the case of Fig. 10(b), since the pulse width of a segment signal to be outputted is 3 (PW = 3), the fineness becomes discrete values such as 3, 6, 9, and 12.

[0007] When continuity of gradation control is considered, in the conventional system, as described above, since gradation setting becomes discrete and unevenness occurs, there occurs a number of levels which can not be set through the driving time of the total of the four frames. This means that since control intervals are irregular in the case where gradation control is made stepwise, the tone control becomes partially impossible.

[0008] An object of the present invention is to provide a liquid crystal display circuit which is improved and is capable of solving the foregoing problem in a liquid crystal display device in which tone control of a pixel is made by using both a pulse width modulation and a frame modulation.

[0009] In order to solve the foregoing problem, according to the present invention, in a liquid crystal display circuit enabling gradation display of a pixel by using both a pulse width modulation in which a drive pulse width for each segment is changed stepwise and a frame modulation in which the way of outputting a drive pulse is changed stepwise for each of one pair of frames of a display screen, it is controlled for each of the frames of the display screen whether or not a pulse width of a drive signal of each pixel is increased by a minimum fine adjustment width, so that the total density of the one pair of frames has continuity and unevenness does not occur in gradation setting.

[0010] In the above structure, it is also possible to structure such that it is determined by a value of lower plural bits of a gradation pallet whether or not the pulse width of the drive signal of each pixel is increased by the minimum fine adjustment width.

[0011] Embodiments of the present invertion will now be described by way of further example only and with reference to the accompanying drawings, in which:

[0012] Fig. 1 is a block diagram showing an embodiment of a liquid crystal display device according to the present invention.

[0013] Fig. 2 is a detailed circuit diagram of a reset signal generating circuit shown in Fig. 1.

[0014] Fig. 3 is a specific circuit diagram of a selecting circuit shown in Fig. 2.

[0015] Fig. 4 is an explanatory diagram for explaining the operation of the selecting circuit shown in Fig. 3.

[0016] Fig. 5 is a detailed circuit diagram of a segment signal generating circuit shown in Fig. 1.

[0017] Fig. 6 is a waveform diagram of segment signals for explaining the operation of a liquid crystal display circuit of Fig. 1.

[0018] Fig. 7 is an explanatory diagram for explaining the operation of the liquid crystal display circuit of Fig. 1.

[0019] Fig. 8 is a waveform diagram showing waveforms of signals of the respective portions of the liquid crystal display circuit shown in Fig. 1.

[0020] Fig. 9 is a signal waveform diagram for explaining a conventional method of gradation control of a liquid crystal display circuit.

[0021] Fig. 10 is a signal waveform diagram for explaining a conventional method of gradation control of

the liquid crystal display circuit.

[0022] Hereafter, an embodiment of the present invention will be described in detail with reference to the drawings.

[0023] Fig. 1 is a block diagram showing an embodiment of a liquid crystal display device according to the present invention.

[0024] A liquid crystal display device 100 is a liquid crystal display device for displaying figures, characters, and the like through a dot matrix display system in a liquid crystal display (LCD) 110.

[0025] The liquid crystal display 110 has such a well-known structure that a liquid crystal is sealed between a pair of transparent glass substrates, a plurality of scanning lines and signal lines are formed in a matrix form on the opposite surfaces of the pair of transparent glass substrates, a display dot made of liquid crystal is formed at each of intersection points of the scanning lines and the signal lines, the scanning lines and the signal lines are sequentially selectively driven by a common driver 120 and a segment driver 130, and an electric charge is stored in the liquid crystal at the sequentially selected intersection point, so that characters and images can be displayed.

[0026] Next, the structure of a display control portion 140 for generating a common signal and a segment signal respectively supplied to the common driver 120 and the segment driver 130 will be described.

[0027] Reference numeral 1 denotes a timing pulse generating circuit (TIMING) which receives a clock pulse CLK supplied from a not-shown clock pulse generator and generates timing pulses PCLK, P0 to P2, S, and R. As shown in Fig. 8, the timing pulse S is a pulse train signal composed of pulses corresponding to common front clock pulses, and the timing pulse R is a 1/2 frequency divided pulse signal of a clock pulse CLK synchronizing with the pulse rising timing of the timing pulse S. The timing pulses P0 to P2 are one pair of pulse signals for indicating any one of gradations of four levels by the pulse width modulation. The timing pulse PCLK is a 1/2 frequency divided pulse signal of the clock pulse CLK synchronizing with the falling timing of the timing pulse S.

[0028] A common counter (COMCNT) 2 for determining the position of a display common is a counter of a predetermined bit number for counting the common clock COMCLK from the timing pulse generating circuit 1, and a frame counter 3 outputs frame signals f0 and f1 for indicating the frame number at that time in two bits in response to an output 2A from the common counter 2. Reference numeral 150 denotes a common signal generating circuit (COMGEN) for outputting a common signal COMD in response to the output from the common counter 2.

[0029] Reference numerals 4 to 7 denote pallets (PALLET) made of registers, or latches, for setting gradation levels to make gradation control. In this embodiment, in order to realize 32 gradations, each pallet is structured to make five bit output, and the four pallets are prepared.

[0030] In each of the pallets 4 to 7, successively from the MSB of the corresponding gradation data, five bits of b4, b3, b2, b1, and b0 are inputted to reset signal generating circuits (RESGEN) 8 to 11. The timing pulses PCLK, P0 to P2, frame signals f1 and f0 are inputted to the reset signal generating circuits 8 to 11, respectively. Each of the reset signal generating circuits 8 to 11 determines at the timing in which the segment signal to be outputted is cut off (negate), and cutoff timing signals RES00, RES01, RES10, and RES11 showing the determination result are inputted to a segment signal generating circuit (SEGGEN) 12.

[0031] Fig. 2 is a detailed circuit diagram of the reset signal generating circuit 8. In Fig. 2, although detailed description will be made on the basis of the structure of the reset signal generating circuit 8, other reset signal generating circuits 9, 10 and 11 have also the same structure.

[0032] Reference numeral 14 denotes a line decoder for decoding the upper three bit data b4, b3, and b2 in the five bit data from the pallet 4 and making effective one of outputs 0 to 7. The other line decoder 13 decodes the timing pulses P2, P1 and P0 from the timing pulse generating circuit 1, and the corresponding output in its eight outputs is made "H". The timing pulse generating circuit 1 responds to the clock pulse CLK, and the timing pulses P2, P1, and P0 are steadily counted, so that the line decoder 13 sequentially scans the outputs 0 to 7.

[0033] Each output of the line decoder 13 and each output of the line decoder 14 take logical product of corresponding outputs by AND gates AND0 to AND7. and when the output of any one of the AND gates AND0 to AND7 becomes "H", the output of an OR gate 16 becomes "H" and a reset signal RESET is generated. If control of only the pulse width moculation is made, the output of the OR gate 16 follows a passage A, and generates a cutoff timing signal RES11 at the output of an AND-OR gate 18.

[0034] In the case where the frame modulation is also used, in order to realize the continuity in gradation, there is prepared a passage B for delaying the reset signal RESET in the case ot the passage A with the aid of a D-type flip-flop 17 by one pulse of the timing pulse PCLK. In the case where the passage B is selected, the pulse width of the segment signal becomes large by one pulse of the timing pulse PCLK.

[0035] Reference numeral 15 denotes a selecting circuit (PWD) for outputting a selection signal 15A to select one of the passages A and B. The selecting circuit 15 makes the selection signal 15A "L" or "H" in response to the frame signals f0 and f1 indicating the frame number at that time, and data b1 and b0 of the lower two bits from the pallet 4 to determine into which frame of one pair of four frames FI to F4 the wide segment signal is inserted. When the selection signal 15A is in the "L" level, the passage A is selected, and when the

selection signal 15A is in the "H" level, the passage B is selected.

[0036] Fig. 3 is a specific circuit diagram of the selecting circuit 15, and Fig. 4 shows the function of the selecting circuit 15. In Fig. 3, reference numerals 151 to 154 denote inverters, 155 to 157 denote AND gates, and 19 denotes an OR gate. As shown in Fig. 4, it is understood that the selection signal 15A to determine the passage A or the passage B for each of the continuous frames (flfO = 00, 01, 10, 11) is outputted by the data bl and b0 of the lower two bits from the pallet 4.

[0037] According to the circuit of Fig. 3, it is structured such that when the data bl and b2 of the lower two bits of the output from the pallet 4 is 00, there is no passage B (only passage A), when 01, the passage B is selected only one time, and when 10, the passage B is selected two times. When the passage B is selected two times in these four frames, It is preferable not to select the passage B in the continuous frames but to select the passage B every other frame. This is because when control is made as dispersedly as possible, there is an effect to reduce a flicker of a screen. When the data bl and b0 of the lower two bits of the output of the pallet 4 is 11, the passage B is selected in three frames.

[0038] Like this, the reset signal generating circuit B is structured such that the basic pulse width of the segment signal is determined by the data contents of the upper three bits of the pallet 4, and it is determined by the data contents of the lower two bits of the pallet 4 whether or not the basic pulse width is added with the minimum control width for each frame. By this, a circuit structure in which both the pulse width control and the control for each frame are used is realized.

[0039] The reset signal generating circuits 9 to 11 provided correspondingly to the outputs of the other pallets 5 to 7 have the same operation, and the cutoff timing signals RES11 to RES00 obtained as the result of this are inputted to the segment signal generating circuit 12.

[0040] Fig. 5 is a detailed circuit diagram of the segment signal generating circuit 12.

[0041] The Q-output of a latch circuit 25 constituted by an R-S flip-flop becomes a segment signal SEG1. Thus, when the timing pulse S is inputted to the set (S) side of the latch circuit 25, the corresponding segment is turned ON, and when a strobe signal of the timing pulse R is inputted to the reset (R) side, the corresponding segment is turned OFF.

[0042] As is understood from Fig. 8, the timing pulse S is outputted at the timing of the front of each common signal without fail. On the other hand, since a signal made of the timing pulse R is outputted at various timings, this changes a segment drive time. Reference characters "a" and "b" of Fig. 5 denote data given from a display RAM 160 and indicating by which gradation of the four kinds the pixel is displayed. If the gradation control is for four colors, two signals are sufficient, and if for black and white, one signal is sufficient. AND gates 20 to 23 are decode outputs of the data "a" and "b", and decodes ab = 00, 01, 10, and 11.

[0043] Since any one of the AND gates 20 to 23 is turned ON, any one of the cutoff timing signals RES00, RES01, RES10, or RES11 is selected as an effective signal by the AND gates 20A to 23A, and a signal in which the OR gate 24 is made to a strobe is formed. Thus, the cutoff timing signals RES00 to RES11 determine a pulse width timing to determine each gradation of four colors.

[0044] Since the display control portion 140 is structured as described above, as shown in Fig. 7, in the case where the output b0 to b4 of five bits from each of the pallets 4 to 7 indicates any one density of 32 stages, the basic pulse width (PW) of the segment signal is set to any of 0 to 7 by using the data (b4, b3, and b2) of the upper three bits. Specifically, judgement is made by the line decoder 14 shown in Fig. 2. The reset signal RESET Is outputted on the basis of the output of this line decoder 14, and the basic pulse width Is determined. On the other hand, in order to determine the increase amount of pulse width for each of one pair of four frames which use the same basic pulse width PW, the selecting circuit 15 uses data (b1 and b0) of the lower two bits from the pallet 4 and the frame signals f1 and f0, and determines the passage of the reset signal RESET to A or B as shown in Fig. 4.

[0045] As a result, as shown in Fig. 6, the width of the segment signal appearing every four frames constituting one pair is increased by one pulse of the timing pulse PCLK according to data of 32 gradations. Although Fig. 6 shows only two cases of PW = 1 and PW = 3, even in the case other than this, in quite the same way, it is increased by one pulse of the timing pulse PCLK.

[0046] As a result, as shown in Fig. 7, to 32 gradations determined in the pallets, conventionally, although only discrete gradation can be obtained and lacks in continuity, according to the structure of Fig. 1, as shown in Fig. 6, continuity is achieved as the total density of four frames constituting one pair, and any one density among continuous gradations of 0 to 31 can be selected.

[0047] According to the present invention, as described above, it is controlled for each frame of a display screen whether or not a pulse width of a drive signal of each pixel is increased by a minimum fine adjustment width, so that it is possible to make continuous gradation control in correspondencewith gradations continuously set in a pallet. Thus, a high quality tone image can be displayed, and the display quality of a tone image with a liquid crystal can be extremely improved.

[0048] Besides, such a structure is made that it is determined by the value of lower plural bits of a gradation pallet whether or not the pulse width of a drive signal of each pixel is increased by a minimum fine adjustment width, so that it is possible to easily make gradation control of gray levels in correspondence with gradation elements by output data of the pallet.

Claims

1. A liquid crystal display circuit enabling gradation display of a pixel by using both a pulse width modulation in which a drive pulse width for each segment is changed stepwise and a frame modulation in which a way of outputting a drive pulse is changed stepwise for each of one pair of frames of a display screen, the liquid crystal display circuit being such that it is controlled for each of the frames of the display screen whether or not a pulse width of a drive signal of each pixel is increased by a minimum fine adjustment width, so that total density of the one pair of frames has continuity and unevenness does not occur in gradation setting.

2. A liquid crystal display circuit according to claim 1, wherein it is determined by a value of lower plural bits of a gradation pallet whether or not the pulse width of the drive signal of each pixel is increased by the minimum fine adjustment width.

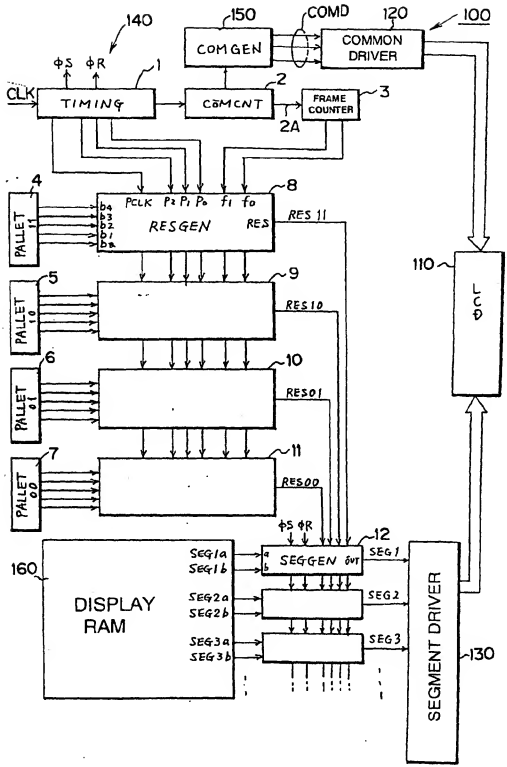

Fig.1

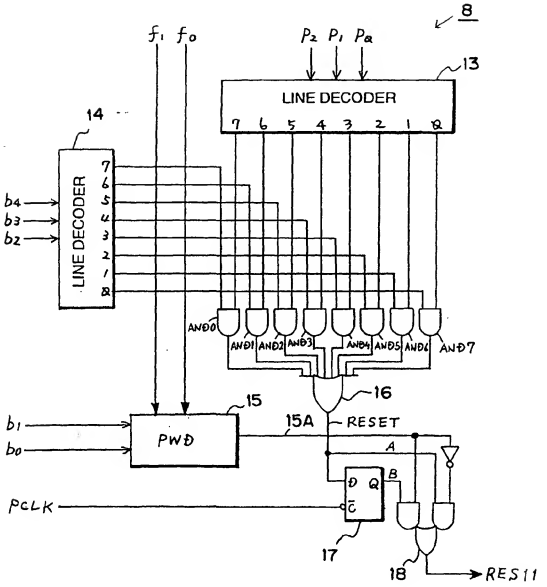

Fig.2

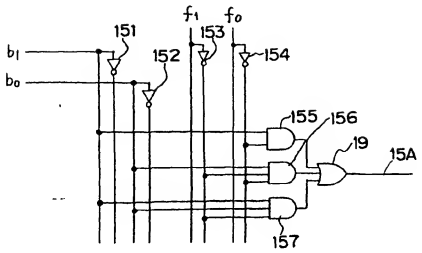

Fig.3

PALLET-DATA					FRAME		PWD	
b4	b3	b2	b1	b0	f1	f0	OUT	AorB
			0	0	0	0	0	A
					0	1	0	A
					1	0	0	A
					1	1	0	A
			0	1	0	0	1	B
					0	1	0	A
					1	0	0	A
					1	1	0	A
			1	0	0	0	1	B
					0	1	0	A
					1	0	1	B
					1	1	0	A
			1	1	0	0	1	B
					0	1	1	B
					1	0	1	B
					1	1	0	A

Fig.4

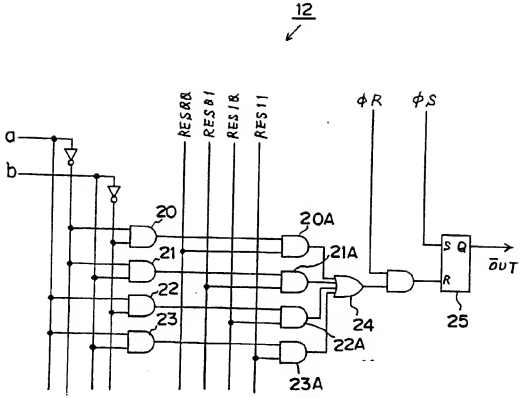

Fig.5

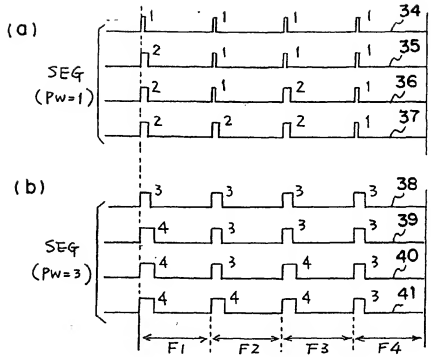

Fig.6

PALLET-DATA					GRAY-LEVEL		
PW			FRM		PW	PW-total	
b4	b3	b2	b1	b0		CONVENTION	INVENTION
0	0	0	0	0	0	0	0
0	0	0	0	1		0	1
0	0	0	1	0		0	2
0	0	0	1	1		0	3
0	0	1	0	0	1	1	4
0	0	1	0	1		2	5
0	0	1	1	0		3	6
0	0	1	1	1		4	7
0	1	0	0	0	2	2	8
0	1	0	0	1		4	9
0	1	0	1	0		6	10
0	1	0	1	1		8	11
0	1	1	0	0	3	3	12
0	1	1	0	1		6	13
0	1	1	1	0		9	14
0	1	1	1	1		12	15
1	0	0	0	0	4	4	16
1	0	0	0	1		8	17
1	0	0	1	0		12	18
1	0	0	1	1		16	19
1	0	1	0	0	5	5	20
1	0	1	0	1		10	21
1	0	1	1	0		15	22
1	0	1	1	1		20	23
1	1	0	0	0	6	6	24
1	1	0	0	1		12	25
1	1	0	1	0		18	26
1	1	0	1	1		24	27
1	1	1	0	0	7	7	28
1	1	1	0	1		14	29
1	1	1	1	0		21	30
1	1	1	1	1		28	31
						11	
						13	
						17	
						19	
					LEVEL-LESS	22	
						23	NONE
						25	
						26	
						27	
						29	
						30	
						31	

Fig.7

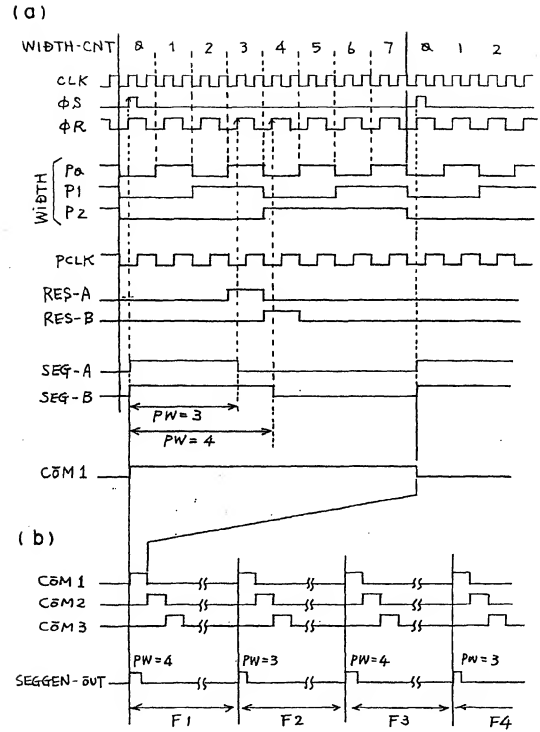

Fig.8

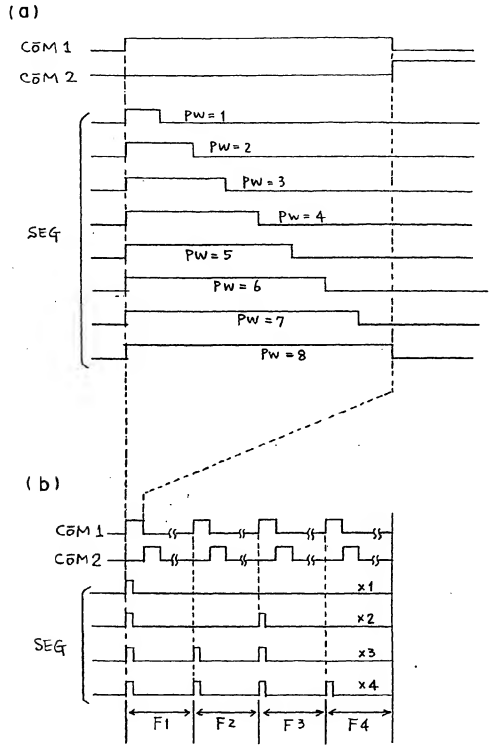

Fig.9

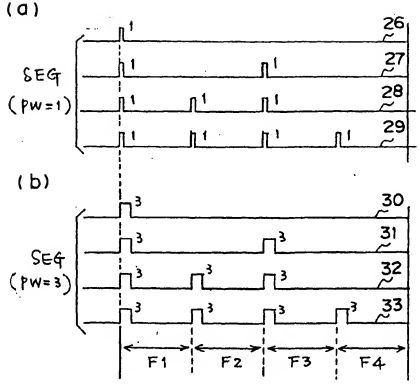

Fig.10

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 5537

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	GB 2 164 190 A (CASIO COMPUTER CO LTD) 12 March 1986 (1986-03-12) * page 2, line 120 - page 3, line 67; figures 2,3,5 *	1,2	G09G3/36
X	US 5 745 087 A (TOMIYOSHI AKIRA ET AL) 28 April 1998 (1998-04-28) * column 11, line 14 - column 12, line 14 *	1	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
			G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	16 November 1999	Amian, D

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 30 5537

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

16-11-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2164190 A	12-03-1986	JP 1926656 C	25-04-1995
		JP 6057059 B	27-07-1994
		JP 61234673 A	18-10-1986
		JP 1934237 C	26-05-1995
		JP 6057058 B	27-07-1994
		JP 61060089 A	27-03-1986
		DE 3531210 A	13-03-1986
		US 4775891 A	04-10-1988
US 5745087 A	28-04-1998	JP 7318903 A	08-12-1995

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82